



## ST. VINCENT PALLOTTI COLLEGE OF ENGINEERING & TECHNOLOGY, NAGPUR

(An autonomous institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

### M. Tech. Scheme of Examination & Syllabus 2026-27

#### EMBEDDED SYSTEM AND VLSI DESIGN

#### SEMESTER II

| Sr. No.      | Course Code | Course Title                                     | Hours per Week |          |           | Credits   | Maximum Marks              |                                |             | Min. Passing Marks | ESE Duration (Hrs.) |
|--------------|-------------|--|----------------|----------|-----------|-----------|----------------------------|--------------------------------|-------------|--------------------|---------------------|
|              |             |  | L              | T        | P         |           | Continuous Assessment (CA) | End Semester Examination (ESE) | Total Marks |                    |                     |
| 1            | 26ES201T    | Digital IC Design                                | 4              | –        | –         | 4         | 40                         | 60                             | 100         | 50                 | 3                   |
| 2            | 26ES201P    | Digital IC Design Lab                            | –              | –        | 2         | 1         | 25                         | 25                             | 50          | 25                 | –                   |
| 3            | 26ES202T    | AI and Machine Learning for Embedded Systems     | 4              | –        | –         | 4         | 40                         | 60                             | 100         | 50                 | 3                   |
| 4            | 26ES202P    | AI and Machine Learning for Embedded Systems Lab | –              | –        | 2         | 1         | 25                         | 25                             | 50          | 25                 | –                   |
| 5            | 26ES203T    | System Verilog                                   | 4              | –        | –         | 4         | 40                         | 60                             | 100         | 50                 | 3                   |
| 6            | 26ES204T    | Program Elective – II                            | 4              | –        | –         | 4         | 40                         | 60                             | 100         | 50                 | 3                   |
| 7            | 26ES205T    | Program Elective – III                           | 4              | –        | –         | 4         | 40                         | 60                             | 100         | 50                 | 3                   |
| 8            | 26ES206T    | Project – I                                      | –              | –        | 6         | 3         | 50                         | 50                             | 100         | 50                 | –                   |
| <b>Total</b> |             |  | <b>20</b>      | <b>–</b> | <b>10</b> | <b>25</b> | <b>300</b>                 | <b>400</b>                     | <b>700</b>  | <b>–</b>           | <b>15</b>           |

| Program Elective – II |   |
|-----------------------|---|
| 26ES204T(i)           | Automotive Embedded Systems               |
| 26ES204T(ii)          | Testing and Verification of VLSI Circuits |

| Program Elective – III |                               |
|------------------------|-------------------------------|
| 26ES205T(i)            | Embedded Systems for robotics |
| 26ES205T(ii)           | AI for VLSI                   |

|                |                  |                 |         |                           |
|----------------|------------------|-----------------|---------|---------------------------|
|                |                  | June 2026       | 1.0     | Applicable for<br>2026-27 |
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**SECOND SEMESTER**

| Course Code | Course Name       | Th | Tu | Pr | Credits | Evaluation |     |       |
|-------------|-------------------|----|----|----|---------|------------|-----|-------|
|             |                   |    |    |    |         | CA         | ESE | Total |
| 26ES201T    | Digital IC Design | 4  | -  | -  | 4       | 40         | 60  | 100   |

| Course Objectives  | Course Outcomes   |
|--|---|
| <p><b>This course is intended to,</b></p> <ol style="list-style-type: none"> <li>1. Understand CMOS digital IC fundamentals and logic gate design.</li> <li>2. Analyse power, delay, and timing behaviour of digital circuits.</li> <li>3. Study advanced combinational and dynamic CMOS logic techniques.</li> <li>4. Design reliable sequential and low-power digital circuits.</li> </ol> | <p><b>After completing this course, students will be able to:</b></p> <ol style="list-style-type: none"> <li>1. Analyze CMOS logic gates and inverter performance.</li> <li>2. Evaluate power, delay, and timing in digital ICs.</li> <li>3. Design combinational and dynamic CMOS circuits.</li> <li>4. Design sequential and low-power digital circuits.</li> </ol> |

|  |                  |
|--|------------------|
| <b>UNIT-I: MOSFET Fundamentals for Digital IC Design</b>   | <b>[12 Hrs.]</b> |
| Review of MOS device physics, MOSFET I-V characteristics, Threshold voltage, body effect, Short-channel effects, MOS fabrication overview.   |                  |
| <b>UNIT-II: CMOS Inverter Analysis</b>   | <b>[12 Hrs.]</b> |
| CMOS inverter operation, DC characteristics and noise margins, Switching characteristics, Propagation delay, Power dissipation (static & dynamic), Effect of sizing and load capacitance |                  |
| <b>UNIT-III: CMOS Combinational Logic Circuits</b>   | <b>[12 Hrs.]</b> |
| Static CMOS logic styles, Pseudo-NMOS logic, Pass transistor logic, Transmission gates, Dynamic logic, Domino logic, Logic sizing and optimization                                       |                  |
| <b>UNIT-IV: Sequential Logic Circuits</b>  | <b>[12 Hrs.]</b> |
| Latches and flip-flops, Static vs dynamic storage elements, Timing parameters: setup, hold, clock skew, Registers and shift registers, Clocking strategies                               |                  |
| <b>UNIT-V: Memory and Interconnect Design</b>  | <b>[12 Hrs.]</b> |
| SRAM cell design, ROM and PLA basics, Memory read/write operations, Interconnect modelling delay, and crosstalk. Clock distribution networks   |                  |

**Text Books**

| S.N | Title   | Authors                       | Edition | Publisher   |
|-----|---|-------------------------------|---------|-------------|
| 1   | CMOS Digital Integrated Circuits: Analysis and Design | Sung-Mo Kang, Yusuf Leblebici | 3rd     | McGraw-Hill |
| 2   | Digital Integrated Circuits: A Design Perspective     | Jan M. Rabaey                 | 2nd     | Pearson     |

**Reference Books**

| S.N | Title  | Authors                       | Edition | Publisher |
|-----|--|-------------------------------|---------|-----------|
| 1   | CMOS VLSI Design: A Circuits and Systems Perspective | Neil H.E. Weste, David Harris | 4th     | Pearson   |
| 2   | Digital Integrated Circuits: A Design Perspective    | Jan M. Rabaey                 | 1st     | Pearson   |

|                |                  |                 |         |                           |
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### EMBEDDED SYSTEM AND VLSI DESIGN

#### SECOND SEMESTER

| Course Code | Course Name           | Th | Tu | Pr | Credits | Evaluation |     |       |
|-------------|-----------------------|----|----|----|---------|------------|-----|-------|
|             |                       |    |    |    |         | CA         | ESE | Total |
| 26ES201P    | Digital IC Design Lab | -  | -  | 2  | 1       | 25         | 25  | 50    |

| Course Objectives   | Course Outcomes   |
|---|---|
| <p><b>This course is intended to,</b></p> <ol style="list-style-type: none"> <li>Understand CMOS digital IC behavior through design and simulation using Microwind.</li> <li>Analyze performance parameters such as power, delay, and noise margins of digital circuits.</li> <li>Design and optimize combinational and sequential CMOS circuits.</li> <li>Apply low-power design techniques in digital ICs.</li> </ol> | <p><b>After completing this course, students will be able to:</b></p> <ol style="list-style-type: none"> <li>Design and simulate basic CMOS logic circuits using Microwind.</li> <li>Analyze power, delay, and timing characteristics of digital ICs.</li> <li>Design combinational and sequential circuits and verify their functionality.</li> <li>Implement optimization and low-power techniques in CMOS circuit design.</li> </ol> |

| S.No | List of Experiments                                       |
|------|---|
| 1    | CMOS inverter design and analysis                         |
| 2    | Buffer design and delay optimization using logical effort |
| 3    | CMOS NAND and NOR gate design and performance analysis    |
| 4    | CMOS XOR gate design                                      |
| 5    | Pass transistor logic and transmission gate design        |
| 6    | Dynamic CMOS and domino logic design                      |
| 7    | Latch and flip-flop design and timing analysis            |
| 8    | Low-power CMOS circuit design and analysis                |

#### Text Books

| S.N | Title   | Authors                       | Edition | Publisher   |
|-----|---|-------------------------------|---------|-------------|
| 1   | CMOS Digital Integrated Circuits: Analysis and Design | Sung-Mo Kang, Yusuf Leblebici | 3rd     | McGraw-Hill |
| 2   | Digital Integrated Circuits: A Design Perspective     | Jan M. Rabaey                 | 2nd     | Pearson     |

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|-----|--|-------------------------------|---------|-----------|
| 1   | CMOS VLSI Design: A Circuits and Systems Perspective | Neil H.E. Weste, David Harris | 4th     | Pearson   |
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|-------------|--------------------------------|----|----|----|---------|------------|-----|-------|
|             |                                |    |    |    |         | CA         | ESE | Total |
| 26ES202T    | AI and ML for Embedded Systems | 4  | -  | -  | 4       | 40         | 60  | 100   |

| Course Objectives  | Course Outcomes  |
|--|--|
| <p><b>This course is intended to,</b></p> <ol style="list-style-type: none"> <li>To introduce the fundamental concepts of machine learning and their relevance to embedded and resource-constrained systems. • To enable learners to acquire, preprocess, and engineer features from sensor and audio data for embedded ML applications.</li> <li>To provide knowledge of neural network models, training strategies, and evaluation techniques suitable for embedded platforms.</li> <li>To develop practical skills in deploying machine learning models on microcontrollers for motion and audio-based applications.</li> <li>To equip learners with the ability to design and optimize complete embedded ML systems considering power, memory, and latency constraints.</li> </ol> | <p><b>After successful completion of the course, students will be able to:</b></p> <ol style="list-style-type: none"> <li>Explain the embedded machine learning pipeline and challenges in constrained hardware environments.</li> <li>Collect, preprocess, and extract meaningful features from real-world sensor and audio data.</li> <li>Design, train, and evaluate neural network models suitable for embedded deployment.</li> <li>Implement motion recognition and audio keyword spotting applications on embedded platforms.</li> <li>Optimize and integrate embedded ML systems by balancing accuracy, resource usage, and power consumption. Estimate interconnect delay/power and apply repeaters/spacing to meet targets.</li> </ol> |

|   |           |
|---|-----------|
| <b>UNIT- I: Foundations of Embedded Machine Learning</b>  | [12 Hrs.] |
| Introduction to machine learning, supervised and unsupervised learning, differences between cloud-based and embedded ML, constraints of embedded hardware, machine learning pipeline, data collection, data preprocessing, feature extraction basics, introduction to embedded ML tools and platforms, ethical considerations in embedded AI. |           |
| <b>UNIT- II : Neural Networks for Embedded Systems</b>  | [12 Hrs.] |
| Basics of neural networks, perceptron model, activation functions, loss functions, training versus inference, underfitting and overfitting, model evaluation metrics, optimization techniques, deployment challenges on microcontrollers, memory and computational constraints.   |           |
| <b>UNIT- III: Time-Series and Motion Classification</b>   | [12 Hrs.] |
| Motion sensor data acquisition, time-series data representation, feature extraction techniques (RMS, FFT, PSD), motion classification pipeline, dataset preparation, training and evaluation of motion classification models, embedded deployment case studies.   |           |
| <b>UNIT- IV: Audio Classification and Keyword Spotting</b>  | [12 Hrs.] |
| Audio signal fundamentals, sampling and framing, feature extraction using MFCCs, convolutional neural networks for audio classification, keyword spotting systems, real-time audio inference on embedded devices, optimization techniques for low-power audio ML.   |           |
| <b>UNIT- V: Advanced Embedded ML Applications and Optimization</b>  | [12 Hrs.] |
| End-to-end embedded ML system design, sensor fusion concepts, model compression and quantization, performance vs power trade-offs, real-world deployment strategies, integration challenges, case studies and project-based learning.   |           |

#### Text Books

| S.N | Title   | Authors                        | Edition     | Publisher      |
|-----|---|--------------------------------|-------------|----------------|
| 1   | TinyML: Machine Learning with TensorFlow Lite on Arduino and Ultra-Low-Power Microcontrollers | Pete Warden, Daniel Situnayake | 1st Edition | O'Reilly Media |
| 2   | Machine Learning for Embedded Systems   | E. López-Aguilera              | 1st Edition | Springer       |

#### Reference Books

| S.N | Title   | Authors                          | Edition     | Publisher |
|-----|---|----------------------------------|-------------|-----------|
| 1   | Introduction to Embedded Systems: A Cyber-Physical Systems Approach | Edward A. Lee, Sanjit A. Seshia. | 3rd Edition | MIT Press |
| 2   | Neural Networks and Deep Learning                                   | Charu C. Aggarwal                | 1st Edition | Springer  |

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| Course Code | Course Name                        | Th | Tu | Pr | Credits | Evaluation |     |       |
|-------------|------------------------------------|----|----|----|---------|------------|-----|-------|
|             |                                    |    |    |    |         | CA         | ESE | Total |
| 26ES202P    | AI and ML for Embedded Systems Lab | -  | -  | 2  | 1       | 25         | 25  | 50    |

| Course Objectives   | Course Outcomes  |
|---|--|
| <p><b>This course is intended</b></p> <ol style="list-style-type: none"><li>To provide hands-on experience in implementing machine learning algorithms on embedded and resource-constrained platforms.</li><li>To enable students to collect, preprocess, and analyze sensor and audio data for embedded machine learning applications.</li><li>To develop practical skills in training, evaluating, and deploying neural network models on microcontrollers.</li><li>To familiarize students with embedded ML tools and workflows inspired by industry practices.</li><li>To enhance problem-solving skills through real-world embedded ML case studies and mini-projects.</li></ol> | <p><b>After successful completion of the course, students will be able to:</b></p> <ol style="list-style-type: none"><li>Implement the embedded machine learning pipeline from data acquisition to deployment</li><li>Extract meaningful features from motion and audio sensor data.</li><li>Train and evaluate lightweight neural network models suitable for embedded systems.</li><li>Deploy and test embedded ML applications such as motion recognition and keyword spotting.</li><li>Optimize embedded ML models considering memory, power, and latency constraints.</li></ol> |

| S.No | List of Experiments  |
|------|--|
| 1    | Introduction to Embedded Machine Learning tools and platforms; installation and setup of Edge Impulse / TensorFlow Lite Micro environment. |
| 2    | Data acquisition and preprocessing using motion sensors (accelerometer/gyroscope); dataset labeling and visualization.                     |
| 3    | Feature extraction from time-series sensor data (RMS, FFT, PSD) and analysis of feature relevance.   |
| 4    | Design, training, and evaluation of a motion classification model using extracted features.  |
| 5    | Deployment of motion classification model on a microcontroller and real-time inference testing.  |
| 6    | Audio data acquisition and preprocessing; extraction of MFCC features for embedded audio applications.                                     |
| 7    | Design and training of an audio classification / keyword spotting neural network model.  |
| 8    | Deployment and performance evaluation of audio classification model on embedded hardware.  |

#### Text Books

| S.N | Title   | Authors           | Edition     | Publisher        |
|-----|---|-------------------|-------------|------------------|
| 1   | Embedded systems Architecture, Programming and Design | Raj Kamal         | 2011        | TMH Publications |
| 2   | Machine Learning for Embedded Systems                 | E. López-Aguilera | 1st Edition | Springer         |

#### Reference Books

| S.N | Title                             | Authors           | Edition     | Publisher            |
|-----|-----------------------------------|-------------------|-------------|----------------------|
| 1   | Embedded System Design            | Steve Heath       |             | Neuwans Publications |
| 2   | Embedded Machine Learning: TinyML | Harald Sundmaeker | 1st Edition | Springer             |

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**SECOND SEMESTER**

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|-------------|----------------|----|----|----|---------|------------|-----|-------|
|             |                |    |    |    |         | CA         | ESE | Total |
| 26ES203T    | System Verilog | 4  | -  | -  | 4       | 40         | 60  | 100   |
|             |                |    |    |    |         |            |     |       |

| Course Objectives  | Course Outcomes  |
|--|--|
| <p><b>This course is intended to,</b></p> <p>Provide in-depth knowledge of SystemVerilog language constructs, enable students to model RTL, testbenches, and verification environments, introduce assertion-based verification and constrained random testing, and prepare students for industry-standard verification methodologies..</p> | <p><b>After successful completion of the course, students will be able to:</b></p> <ol style="list-style-type: none"><li>1. Explain SystemVerilog language features and design concepts.</li><li>2. Develop synthesizable RTL models using SystemVerilog</li><li>3. Design testbenches with OOP constructs</li><li>4. Apply assertions and functional coverage for verification</li><li>5. Build constrained-random verification environments.</li></ol> |

|  |                  |
|--|------------------|
| <b>UNIT- I: Introduction to SystemVerilog</b>  | <b>[12 Hrs.]</b> |
| Evolution from Verilog to SystemVerilog, design versus verification constructs, compilation units and packages, data types such as logic, bit, byte, int, shortint and longint, arrays including packed, unpacked, dynamic arrays and associative arrays, strings, enumerations, structures and unions.. |                  |
| <b>UNIT-II : RTL Modeling Using SystemVerilog</b>  | <b>[12 Hrs.]</b> |
| Modules and interfaces, always_comb, always_ff and always_latch constructs, parameterized designs, clocking blocks, modports and virtual interfaces, synthesis guidelines and coding best practices.   |                  |
| <b>UNIT-III: Testbench Architecture and OOP Concepts</b>   | <b>[12 Hrs.]</b> |
| Verification versus design hierarchy, classes and objects, inheritance, polymorphism and encapsulation, constructors and methods, mailboxes and events, program blocks, reusable testbench components.   |                  |
| <b>UNIT- IV: Assertions and Functional Coverage</b>  | <b>[12 Hrs.]</b> |
| Immediate versus concurrent assertions, SystemVerilog Assertions (SVA), property and sequence constructs, assertion-based verification, functional coverage, covergroups, coverpoints, bins and crosses, coverage-driven verification.   |                  |
| <b>UNIT-V: Randomization and IPC</b>   | <b>[12 Hrs.]</b> |
| Randomization and constraints, constraint blocks and rand and randc variables, pre-randomize and post-randomize methods, scoreboards and reference models, overview of verification methodologies including UVM basics, industry verification flow and best practices.                                   |                  |

**Text Books**

| S.N | Title   | Authors   | Edition | Publisher |
|-----|---|---|---------|-----------|
| 1   | SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling | Stuart Sutherland, Simon Davidmann, Peter Flake | 2nd     | Springer  |
| 2   | SystemVerilog for Verification: A Guide to Learning the Testbench Language Features       | Chris Spear, Greg Tumbush                       | 3rd     | Springer  |

**Reference Books**

| S.N | Title                                   | Authors  | Edition | Publisher            |
|-----|---|--|---------|----------------------|
| 1   | SystemVerilog Assertions Handbook       | Ben Cohen, Srinivasan Venkataramanan, Ajeetha Kumari, Lisa Piper | 4th     | VhdlCohen Publishing |
| 2   | Writing Testbenches using SystemVerilog | Janick Bergeron  | 2nd     | Springer             |
| 3   | UVM 1.2 User Guide                      | Accellera Systems Initiative                                     | -       | Accellera            |

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|-------------|-----------------------------|----|----|----|---------|------------|-----|-------|
|             |                             |    |    |    |         | CA         | ESE | Total |
| 26ES204T(i) | Automotive Embedded Systems | 4  | -  | -  | 4       | 40         | 60  | 100   |
|             |                             |    |    |    |         |            |     |       |

| Course Objectives   | Course Outcomes   |
|---|---|
| <p><b>This course is intended to,</b></p> <ol style="list-style-type: none"><li>1. Introduce vehicle architectures, ECU roles, and embedded building blocks with sensor interfacing and networking protocols.</li><li>2. Explain real-time control techniques, scheduling, software integration, and verification loops in automotive systems.</li><li>3. Explore functional safety, cybersecurity, compliance requirements, and testing frameworks based on ISO standards.</li><li>4. Cover EV powertrains, AUTOSAR concepts, embedded Linux, and edge computing platforms through hands-on projects and case studies.</li></ol> | <p><b>After successful completion of the course, students will be able to:</b></p> <ol style="list-style-type: none"><li>1. Describe vehicle systems, ECU architecture, sensor interfacing, and in-vehicle communication protocols.</li><li>2. Apply control algorithms, scheduling techniques, and verification frameworks in embedded automotive software.</li><li>3. Design and analyze safety and security mechanisms using standards such as ISO 26262 and implement compliance strategies.</li><li>4. Integrate EV control systems, AUTOSAR-based architectures, and embedded Linux platforms for edge applications with proper validation.</li></ol> |

|   |                  |
|---|------------------|
| <b>UNIT- I: Vehicle E/E Architecture &amp; ECU Fundamentals</b>   | <b>[12 Hrs.]</b> |
| Vehicle subsystems and E/E architecture; ECU roles, constraints, and real-time requirements; overview of automotive embedded systems.                                 |                  |
| <b>UNIT-II : Embedded Hardware &amp; In-Vehicle Networking</b>  | <b>[12 Hrs.]</b> |
| Embedded hardware basics (MCU/SoC, memory, sensors, EMC/EMI); in-vehicle communication protocols (CAN, LIN, FlexRay, Ethernet); automotive diagnostics (UDS, OBD-II). |                  |
| <b>UNIT-III: Real-Time Control &amp; Embedded Software</b>  | <b>[12 Hrs.]</b> |
| Automotive control concepts and PID control; real-time embedded software (scheduling, ISRs, DMA, watchdogs, OTA); model-based design and verification (MIL/SIL/HIL).. |                  |
| <b>UNIT- IV: Functional Safety &amp; Automotive Cybersecurity</b>   | <b>[12 Hrs.]</b> |
| ISO 26262 safety lifecycle and ASIL; safety mechanisms and compliance documentation; automotive cybersecurity fundamentals and secure ECU design.                     |                  |
| <b>UNIT-V: Electrified Vehicles, AUTOSAR &amp; Edge Platforms</b>   | <b>[12 Hrs.]</b> |
| EV powertrain systems and diagnostics; AUTOSAR Classic & Adaptive platforms; Embedded Linux for automotive applications; system validation and OTA updates.           |                  |

#### Text Books

| S.N | Title   | Authors                               | Edition | Publisher                   |
|-----|---|---------------------------------------|---------|-----------------------------|
| 1   | Automotive Embedded Systems Handbook                      | Nicolas Navet, Francoise Simonot-Lion | Latest  | CRC Press                   |
| 2   | Automotive Embedded Systems for Engineers                 | Andrew K. Shepherd                    | 1st     | Elsevier / Academic Press   |
| 3   | Embedded Software Development for Safety-Critical Systems | Chris Hobbs                           | Latest  | Springer / Wiley-IEEE Press |

#### Reference books

| S.N | Title  | Authors                   | Edition | Publisher                    |
|-----|--|---------------------------|---------|------------------------------|
| 1   | Automotive Ethernet – The Definitive Guide   | Bob Metcalfe              | Latest  | O'Reilly Media               |
| 2   | Functional Safety for Road Vehicles: New Challenges and Solutions for E-Mobility and Automated Driving | Hans-Leo Ross             | 1st     | Springer / SAE International |
| 3   | Automotive Control Systems: For Engine, Driveline, and Vehicle   | Uwe Kiencke, Lars Nielsen | 2nd     | Springer                     |

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|--------------|----------------------|----|----|----|---------|------------|-----|-------|
|              |                      |    |    |    |         | CA         | ESE | Total |
| 26ES205T(ii) | PE – III AI for VLSI | 4  | -  | -  | 4       | 40         | 60  | 100   |

| Course Objectives   | Course Outcomes  |
|---|--|
| <p><b>The objectives of this course are to:</b></p> <ol style="list-style-type: none"> <li>1. Introduce the basic concepts of Artificial Intelligence, Machine Learning, and Deep Learning relevant to VLSI systems.</li> <li>2. Explain how different types of VLSI data such as RTL, netlists, layouts, timing, and manufacturing data are represented and analyzed using AI.</li> <li>3. Familiarize students with the application of AI techniques in early design estimation, physical design, and verification stages of VLSI.</li> <li>4. Provide an understanding of how AI assists in improving Quality of Results (QoR), including power, performance, and area metrics.</li> <li>5. Create awareness about the limitations, reliability, and ethical considerations of using AI in VLSI design and semiconductor manufacturing.</li> </ol> | <p><b>After successful completion of the course, students will be able to:</b></p> <ol style="list-style-type: none"> <li>1. Explain the fundamental concepts of AI, ML, and DL and their relevance to VLSI design and EDA workflows.</li> <li>2. Identify different types of VLSI data and describe their representations used in AI-based analysis.</li> <li>3. Describe the use of AI techniques for early QoR estimation and physical design optimization.</li> <li>4. Interpret the role of AI in verification, timing analysis, yield improvement, and testing processes.</li> <li>5. Evaluate the benefits, limitations, and ethical issues associated with AI-assisted VLSI design and manufacturing.</li> </ol> |

|   |           |
|---|-----------|
| <b>UNIT- I: Foundations of AI for VLSI</b>  | [12 Hrs.] |
| Basics of Artificial Intelligence, Machine Learning, and Deep Learning, Concept of data, datasets, and data splitting, Overfitting and underfitting (basic idea), Simple performance metrics used in AI, Types of VLSI data and their representation, Basic idea of feature selection and feature learning, Interpretation of AI results, Limitations and bias in AI systems. |           |
| <b>UNIT- II : AI for Front-End &amp; Early QoR</b>  | [12 Hrs.] |
| Concept of Quality of Results (QoR), Power, Performance, and Area (PPA) metrics, Need for early QoR estimation, Use of simple AI models for early estimation, RTL and netlist parameters for prediction, Early floorplanning quality indicators, Concept of surrogate models Reuse of AI models across designs  |           |
| <b>UNIT- III: AI for Physical Design</b>  | [12 Hrs.] |
| Role of AI in physical design, Congestion and routability prediction, Timing risk estimation using AI, AI concepts for layout and netlist analysis, Reinforcement learning idea for placement and routing, AI-assisted ECO suggestions, Verification of AI outputs using sign-off tools   |           |
| <b>UNIT- IV: AI in Verification &amp; Timing</b>  | [12 Hrs.] |
| Challenges in functional verification and timing analysis, AI-based regression analysis and log clustering, Test selection and coverage improvement using AI, Anomaly detection concepts Corner reduction idea for timing analysis, High-level timing and parasitic estimation Case studies in AI-assisted verification   |           |
| <b>UNIT- V: AI for Yield, Test &amp; Manufacturing</b>  | [12 Hrs.] |
| Role of AI in semiconductor manufacturing, Wafer map analysis and defect detection, Yield prediction concepts, Adaptive testing ideas Fault diagnosis using AI, Reliability assessment concepts, Data handling and ethical issues in manufacturing.   |           |

#### Text Books

| S.N | Title  | Authors  | Edition | Publisher  |
|-----|--|--|---------|------------|
| 1   | Advancing VLSI through Machine Learning: Innovations and Research Perspectives | Abhishek N. Tripathi, Jagana B. Padhy, Indrasen Singh, Shubham Tayal, Ghanshyam Singh (Eds.) | 1st     | CRC Press. |
| 2   | Machine Learning Applications in Electronic Design Automation                  | Haoxing Ren, Jiang Hu (Eds.)   | 1st     | Springer.  |

#### Reference Books

| S.N | Title  | Authors  | Edition | Publisher              |
|-----|--|--|---------|------------------------|
| 1   | Electronic Design Automation for Integrated Circuits Handbook (2-Vol. set) | Luciano Lavagno, Louis Scheffer, Grant Martin (Eds.) | 1st     | CRC Press / Routledge. |
| 2   | Hands-On Machine Learning with Scikit-Learn, Keras, and TensorFlow         | Aurélien Géron                                       | 3rd     | O'Reilly               |

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| Chairman - BoS | Dean – Academics | Date of Release | Version |                        |