ST. VINCENT PALLOTTI COLLEGE OF ENGINEERING & TECHNOLOGY, NAGPUR

(An autonomous institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

M. Tech. Scheme of Examination & Syllabus 2025-26

EMBEDDED SYSTEM AND VLSI DESIGN

SEMESTER I

Sr. No.	CourseCode	Course Title	Hours Per Week			Credits	Maximum Marks			Minimum Passing Marks	Duration of ESE (Hours)
			L	T	P		Continual Assessment	End Sem Examination	Total		
1.	25ES101T	Embedded System Design and RTOS	4	-	-	4	40	60	100	50	3
2.	25ES101P	Embedded System Design and RTOS Lab	-	-	2	1	25	25	50	25	-
3.	25ES102T	Analog and Digital VLSI Design	4	-	-	4	40	60	100	50	3
4.	25ES102P	Analog and Digital VLSI Design Lab		-	2	1	25	25	50	25	-
5.	25ES103T	VLSI Testing	4	-	-	4	40	60	100	50	3
6.	25ES104T	Industry 4.0 and Industrial IoT*	-	-		4	40	60	100	50	3
7.	25ES105T	Program Elective – I	4	-	-	4	40	60	100	50	3
8.	25ES106P	Technical Seminar	-	-	6	3	100	-	100	50	2
Total			16	-	10	25	350	350	700	-	-

*Course to be conducted online through NPTEL. The course will be notified one month prior to the commencement of the semester.

Program Elective Basket

Program Elective – I	
25ES105T(i)	ASIC Design
25ES105T(ii)	Robotics and Automation

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EMBEDDED SYSTEM AND VLSI DESIGN

FIRST SEMESTER

Course Code	Course Name	Th	Tu	Pr	Credits	Evaluation		
						CA	ESE	Total
25ES101T	Embedded System Design and RTOS	4	-	-	4	40	60	100

Course Objectives	Course Outcomes
This course is intended 1. Introduce the fundamentals of embedded systems, their characteristics, and design challenges. 2. Provide knowledge of processors, memory, peripherals, and interfacing techniques. 3. Enable students to apply RTOS features for designing real-time embedded applications through case studies.	Student will be able to • Explain embedded system architecture, challenges, and design flow. • Interface peripherals and develop embedded firmware. • Implement device drivers and interrupt service routines. • Analyze RTOS concepts, scheduling, and synchronization mechanisms. • Apply RTOS in real-world embedded applications and case studies.

UNIT- I: Introduction to Embedded System	**[12 Hrs.]**
Characteristics and quality attributes of embedded systems – Design challenges and design process – Embedded processors: RISC, CISC, ARM, DSP, SoC overview – Memory organization: SRAM, DRAM, Flash, EEPROM, memory mapping – Applications: Consumer, automotive, medical, industrial, IoT	
UNIT–II : Peripherals & Interfacing	**[12 Hrs.]**
GPIO, switches, LEDs, keypads – Timers, counters, PWM, watchdog timers, RTC – ADC/DAC interfacing basics – Serial & parallel communication: UART, SPI, I²C, CAN, USB – Sensor and actuator interfacing with processors	
UNIT–III: Embedded Firmware & Software Design	**[12 Hrs.]**
Embedded C/C++ programming concepts – Device drivers: I/O, timer, ADC, DAC – Interrupt handling and exception handling – Bootloaders and firmware updates – Debugging and testing tools	
UNIT–IV: Real-Time Operating System (RTOS) Concepts	**[12 Hrs.]**
Real-time system basics: hard vs soft real-time, deadlines, latency – RTOS architecture and kernel functions – Task scheduling: static and dynamic – IPC mechanisms: semaphores, mutex, message queues – Context switching, priority inversion, and solutions	
UNIT–V: RTOS Applications & Case Studies	**[12 Hrs.]**
RTOS-based design methodology – RTOS features: FreeRTOS, VxWorks, µC/OS-II, RTLinux – Case studies: Automotive ECU, Medical devices, IoT-based systems – Future trends: Embedded AI, Cyber-Physical Systems, IoT security	

Text Books

S.N	Title	Authors	Edition	Publisher
1	Embedded systems Architecture, Programming and Design	Raj Kamal	2011	TMH Publications
2	Embedded System Design	Frank Vahid	New edition 2001	Wiley Publications

Reference Books

S.N	Title	Authors	Edition	Publisher
1	Embedded System Design	Steve Heath		Neuwans Publications
2	Embedded Real Time Systems Programming	Sriram V Iyer, Pankaj Gupta	2012	Tata McGraw- Hill

		August 2025	1	Applicable for 2025-26
Chairman - BoS	Dean – Academics	Date of Release	Version	

FIRST SEMESTER

Course Code	Course Name	Th	Tu	Pr	Credits	Evaluation		
						CA	ESE	Total
25ES101P	Embedded System Design and RTOS Lab	4	-	-	4	25	25	50

Course Objectives	Course Outcomes
This course is intended 1. Introduce the fundamentals of embedded systems, their characteristics, and design challenges. 2. Provide knowledge of processors, memory, peripherals, and interfacing techniques. 3. Enable students to apply RTOS features for designing real-time embedded applications through case studies.	Student will be able to • Explain embedded system architecture, challenges, and design flow. • Interface peripherals and develop embedded firmware. • Implement device drivers and interrupt service routines. • Analyze RTOS concepts, scheduling, and synchronization mechanisms. • Apply RTOS in real-world embedded applications and case studies.

S.No	List of Experiments
1	Introduction to Embedded Development Environment
2	GPIO and Digital I/O Interfacing
3	Timer and PWM Programming
4	ADC and DAC Interfacing
5	LCD Interfacing
6	RTOS Basics: Task Creation and Scheduling
7	IoT-based Embedded Application (Sensor Data Transmission)
8	Mini Project on RTOS-based Embedded Application

Text Books

S.N	Title	Authors	Edition	Publisher
1	Embedded systems Architecture, Programming and Design	Raj Kamal	2011	TMH Publications
2	Embedded System Design	Frank Vahid	New edition 2001	Wiley Publications

Reference Books

S.N	Title	Authors	Edition	Publisher
1	Embedded System Design	Steve Heath		Neuwans Publications
2	Embedded Real Time Systems Programming	Sriram V Iyer, Pankaj Gupta	2012	Tata McGraw- Hill

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EMBEDDED SYSTEM AND VLSI DESIGN

FIRST SEMESTER

Course Code	Course Name	Th	Tu	Pr	Credits	Evaluation		
						CA	ESE	Total
25ES102T	Analog and Digital VLSI Design	4	-	-	4	40	60	100

Course Objectives	Course Outcomes
1. Build intuition of MOS device behavior and CMOS logic/analog blocks without heavy math. 2. Explain layout fundamentals (design rules, stick diagrams) and link layout choices to delay, power, and matching. 3. Describe timing, power, and interconnect effects for digital paths, and basic memory ideas. 4. Introduce analog building blocks (current mirrors, differential pairs, op-amp basics) and analog layout practices. 5. Familiarize students with Microwind for viewing/editing layouts and doing simple simulations (for demonstrations/practicals).	After successful completion of the course, students will be able to: 1. Explain CMOS inverter/logic behavior, noise margins, and sizing trade-offs. 2. Interpret layout rules and relate layout to delay, power, and matching. 3. Estimate first-order delay/power and discuss interconnect/parasitic impact on timing. 4. Describe key analog blocks and outline good analog layout (matching, common-centroid, guard rings). 5. Review Microwind layout/simulation results and summarize observations in short reports.

UNIT- I: CMOS & Digital Basics	**[12 Hrs]**
MOSFET recap; DC transfer of CMOS inverter; noise margins; switching behavior, logical effort (concept), sizing & fan-out; static/dynamic power; standard CMOS gates (NAND/NOR, transmission gate), multiplexers & arithmetic at gate level.	
UNIT-II : Layout Foundations	**[12 Hrs]**
Stick diagrams, Euler paths; lambda-based design rules; wells, diffusion, poly, contacts, metal; layout of inverter/NAND/NOR/TG; parasitics (Cgd/Cdb, wiring C/R) and impact on delay/power; intro to DRC, layout vs. schematic (concept); reading Microwind rule checks.	
UNIT-III: Timing & Interconnect	**[12 Hrs]**
Path delay notions (rise/fall, effective fan-out); RC models (intuitive Elmore), wire scaling; buffers/repeaters (idea); clocking basics, setup/hold at a high level; glitching & hazards; overview of SRAM bit-cell idea and sense amplifier (concept only).	
UNIT-IV: Analog Building Blocks	**[12 Hrs]**
Current mirrors (basic & cascode—concepts), biasing; differential pair, gain stages, simple op-amp view, bandwidth/compensation (intuitive); common-mode & output swing ideas; resistor/Capacitor basics on chip; matching, gradients; analog layout: common-centroid, dummy devices, guard rings, substrate ties.	
UNIT-V: Mixed-Signal & Practical Considerations	**[12 Hrs]**
I/O pads & ESD (concept), references (bandgap—idea), simple data converter concepts (R-2R DAC, flash ADC high-level), supply/grounding and decoupling; variability & corners (PVT—intuition); documentation & review practices; reading Microwind waveforms and reports.	

Text Books

S.N	Title	Authors	Edition	Publisher
1	CMOS VLSI Design: A Circuits and Systems Perspective	Neil H. E. Weste, David Harris	4th or later	Pearson
2	Design of Analog CMOS Integrated Circuits	Behzad Razavi	1st or later	McGraw-Hill

Reference Books

S.N	Title	Authors	Edition	Publisher
1	Analog Integrated Circuit Design	David Johns, Ken Martin	1st	Wiley
2	CMOS Analog Circuit Design	Phillip E. Allen, Douglas R. Holberg	2nd	Oxford

		August 2025	1	Applicable for 2025-26
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Course Code	Course Name	Th	Tu	Pr	Credits	Evaluation		
						CA	ESE	Total
25ET102P	Analog and Digital VLSI Design Lab	-	-	2	1	25	25	50

Course Objectives	Course Outcomes
1. Use the tools: Get comfortable drawing schematics in DSCH and layouts/DRC in Microwind. 2. Basic cells: Build simple CMOS gates (inverter, NAND, NOR) and know basic sizing ideas. 3. Combine blocks: Put cells together to make a full adder/subtractor, decoder, and 8×1 MUX. 4. Sequential logic: Make latches/flip-flops and a small counter; notice simple timing behaviour.	After successful completion of the course, students will be able to: 1. Create and DRC-clean basic cells (INV/NAND/NOR) and show correct truth-table waveforms. 2. Build FA/FS/Decoder/8×1 MUX and prove they work with simple test waveforms. 3. Implement RS, D, and JK elements and mention setup/hold effects in simple words. 4. Make a 4-bit ripple counter, show the count sequence, and note ripple delay.

Minimum 8 practical based on the syllabus.

Sr. No.	List of the experiment (Minimal deliverables per experiment: DSCH schematic, MICROWIND layout (DRC-clean where applicable), 1–2 key waveforms, and a 3–5 bullet design rationale (sizing/layout choices & observations).
1	Create & validate a CMOS Inverter: design schematic in DSCH, create MICROWIND layout, DRC-clean, and verify transient behaviour vs. a target rise/fall time.
2	Create a 2-input NAND gate cell: schematic + layout; ensure correct logic, DRC-clean layout, and justify sizing for balanced delays.
3	Create a 2-input NOR gate cell: schematic + layout; verify function and compare delay with NAND (brief design rationale).
4	Create a Full Adder: compose from gates/TGs at schematic level, propose a standard-cell style layout for the core logic, verify sum/carry waveforms.
5	Create a Full Subtractor: schematic composition, implement layout for core block, verify borrow/difference, and contrast with Full Adder design.
6	Create a 2-to-4 (or 3-to-8) Decoder: schematic + partial layout of one representative output path; verify truth table and discuss fan-out loading.
7	Create an RS Latch: schematic + compact layout; verify set/reset behaviour and discuss metastability risk qualitatively.
8	Create a D-Latch cell: schematic + layout; DRC-clean and verify transparency/hold behaviour with timing waveforms.
10	Create a JK Flip-Flop (edge-triggered from latches): schematic assembly, show a feasible layout plan, verify state transitions; note setup/hold qualitatively.
11	Create an Asynchronous Counter (e.g., 4-bit ripple): schematic using FFs, floorplan a simple layout for one stage, verify count sequence and discuss ripple delay.
10	Create a Static RAM bit-cell (concept) + read/write path: schematic of 6T cell with simple periphery, sketch/layout the cell, demonstrate read/write waveforms qualitatively.
11	Create an 8×1 Multiplexer: schematic using gates/TGs, layout a representative slice, verify selection timing and discuss input loading.
12	Create a Differential Pair (basic differential amplifier): schematic + matched layout (common-centroid), verify differential transfer qualitatively and comment on matching.

Text Books

S.N	Title	Authors	Edition	Publisher
1	CMOS VLSI Design: A Circuits and Systems Perspective	Neil H. E. Weste, David Harris	4th or later	Pearson
2	Design of Analog CMOS Integrated Circuits	Behzad Razavi	1st or later	McGraw-Hill

Reference Books

S.N	Title	Authors	Edition	Publisher
1	Analog Integrated Circuit Design	David Johns, Ken Martin	1st	Wiley
2	CMOS Analog Circuit Design	Phillip E. Allen, Douglas R. Holberg	2nd	Oxford

Reference Book: Lab Manual

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FIRST SEMESTER

Course Code	Course Name	Th	Tu	Pr	Credits	Evaluation		
						CA	ESE	Total
25ES103T	VLSI Testing	4	-	-	4	40	60	100

Course Objectives	Course Outcomes
1. Understand the need for testing and fault modelling. 2. Develop ability to derive fault lists and efficient test sets. 3. Formulate and implement memory test strategies. 4. Apply IEEE 1149.1 boundary-scan methodology. 5. Design and integrate Built-In Self-Test (BIST).	After successful completion of the course, students will be able to: 1. Analyze the need for fault modeling and testing of digital circuits 2. Generate fault lists for digital circuits and compress the tests for efficiency 3. Create tests for digital memories and analyze failures in them 4. Apply boundary scan technique to validate the performance of digital circuits 5. Design built-in self tests for complex digital circuits

UNIT- I : Fault Modeling & Logic Simulation	**[12 Hrs.]**
Faults in digital circuits : Failures and Faults, Modeling of faults, Temporary Faults. **Logic Simulation :** Applications, Problems in simulation-based design verification, types of simulation, The unknown logic values, compiled simulation, event-driven simulation, Delay models, Element evaluation, Hazard detection, Gate-level event-driven Simulation.	
UNIT-II : Combinational ATPG, Diagnosis & Testable Design	**[12 Hrs.]**
Test generation for Combinational Logic circuits : Fault Diagnosis of digital circuits, Test generation techniques for combinational circuits, Detection of multiple faults in Combinational logic circuits. **Testable Combinational logic circuit design :** The Read-Muller expansion technique, Three level OR-AND-OR design, Automatic synthesis of testable logic.	
UNIT-III: Testable Multilevel Combinational Design & Sequential ATPG	**[12 Hrs.]**
Testable Combinational logic circuit design : Testable design of multilevel combinational circuits, Synthesis of random pattern testable combinational circuits, Path delay fault testable combinational logic design, Testable PLA design. **Test generation for Sequential circuits :** Testing of sequential circuits as Iterative combinational circuits, state table verification, Test generation based on Circuit Structure, Functional Fault models, test Generation based on Functional Fault models.	
UNIT-IV: DFT for Sequential Circuits (Scan, LSSD & Boundary Scan)	**[12 Hrs.]**
Design of testable sequential circuits : Controllability and observability, Ad-Hoc design rules for improving testability, design of diagnosable sequential circuits, the scan-path technique for testable sequential circuit design, Level Sensitive Scan Design (LSSD), Random Access Scan Technique, Partial scan, testable sequential circuit design using Nonscan Techniques, Cross check, Boundary Scan.	
UNIT-V: Built-In Self-Test (BIST) & Memory Testing	**[12 Hrs.]**
Built-In Self Test : Test pattern generation for BIST, Output response analysis, Circular BIST, BIST Architectures. **Testable Memory Design :** RAM Fault Models, Test algorithms for RAMs, Detection of pattern-sensitive faults, BIST techniques for RAM chips, Test generation and BIST for embedded RAMs.	

Text Books

S.N	Title	Authors	Edition	Publisher
1	Digital Circuit Testing and Testability	Lala Parag K	1997	New York, Academic Press
2	Digital Systems Testing and Testable Design	Abramovici M, Breuer M A and Friedman A D	1994	Wiley

Reference Books

S.N	Title	Authors	Edition	Publisher
1	Essential of Electronic Testing for Digital, Memory and Mixed Signal Circuits	Vishwani D Agarwal	2002	Springer
2	VLSI Test Principles and Architectures	Wang, Wu and Wen	2006	Morgan Kaufmann

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FIRST SEMESTER

Course Code	Course Name	Th	Tu	Pr	Credits	Evaluation		
						CA	ESE	Total
25ES104T	Industry 4.0 and Industrial IoT	4	-	-	4	40	60	100

Course Objectives	Course Outcomes
This course is intended 1. Introduce the fundamentals of embedded systems, their characteristics, and design challenges. 2. Provide knowledge of processors, memory, peripherals, and interfacing techniques. 3. Enable students to apply RTOS features for designing real-time embedded applications through case studies.	Student will be able to • Explain Industry 4.0 concepts and the evolution of cyber-physical systems. • Describe IIoT architecture, components, • Describe communication protocols. • Analyze data analytics and machine learning applications in industrial systems. • Design and evaluate real-world Industry 4.0 and IIoT case studies.

UNIT- I: Introduction to Industry 4.0	**[12 Hrs.]**
Evolution of Industrial Revolutions – Key Drivers – Cyber-Physical Systems (CPS) – Smart Manufacturing and Automation – Challenges and Opportunities	
UNIT–II : Industrial Internet of Things (IIoT)	**[12 Hrs.]**
IoT vs IIoT – IIoT Architecture and Components – Sensors, Actuators, and Communication Protocols – Edge and Fog Computing – Security and Privacy in IIoT	
UNIT–III: Communication Technologies for IIoT	**[12 Hrs.]**
Industrial Communication Protocols (Modbus, OPC-UA, MQTT, CoAP) – Wireless Communication – 5G in IIoT – Network Design and Topologies	
UNIT–IV: Data Analytics and Machine Learning in Industry 4.0	**[12 Hrs.]**
Data Acquisition and Processing – Predictive Maintenance – Machine Learning for Industrial Applications – Big Data Analytics – Real-Time Data Processing and Visualization	
UNIT–V: Applications and Case Studies	**[12 Hrs.]**
Smart Factories – Digital Twins – IIoT in Supply Chain – Energy Management – Quality Control – Healthcare & Agriculture Applications – Future Trends	

Text Books

S.N	Title	Authors	Edition	Publisher
1	Industry 4.0: The Industrial Internet of Things	Alasdair Gilchrist	1st	Apress, 2016
2	Introduction to Industrial Internet of Things and Industry 4.0	Sudip Misra	1st	CRC Press, 2021

Reference Books

S.N	Title	Authors	Edition	Publisher
1	Handbook of Maintenance Management and Engineering	Mohamed Ben-Daya, Taghi Duffuaa, et al.	1st	Springer, 2019
2	Building Industrial Internet of Things: Implementing IIoT in Manufacturing	Andrew Minteer	1st	Packt Publishing, 2019

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Course Code	Course Name	Th	Tu	Pr	Credits	Evaluation		
						CA	ESE	Total
25ES105T(i)	Program Elective – I ASIC Design	4	-	-	4	40	60	100

Course Objectives	Course Outcomes
1. Introduce the end-to-end ASIC implementation flow and foundational RTL-to-netlist synthesis. 2. Develop competence to design and evaluate floorplans and power distribution networks. 3. Design/analyze clock distribution to meet skew/latency targets, and to correlate extracted parasitics. 4. Equip students to perform MMMC static timing analysis. 5. Prepare students to analyse physical verification (DRC/LVS) and EM/IR checks, integrate scan/MBIST, and assemble a tape-out package that meets sign-off requirements.	After successful completion of the course, students will be able to: 1. Explain the ASIC flow and synthesize a small RTL block with basic SDC, then interpret area/power/timing reports. 2. Interpret floorplan and power grid, timing-driven placement, and congestion/IR-drop indicators. 3. Analyze a clock tree to skew/latency targets, correlate parasitics with timing. 4. Interpret MMMC STA with OCV/AOCV to diagnose setup/hold and crosstalk impacts and implement targeted timing/power fixes. 5. Analyze DRC/LVS and EM/IR checks, integrate basic scan/MBIST, and assemble a tape-out package meeting sign-off.

UNIT- I: Introduction to ASICs & CMOS Datapath Logic	**[12 Hrs.]**
Introduction to ASICs: Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries. **CMOS Logic:** Data path Logic Cells: Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells, Cell Compilers.	
UNIT–II : ASIC Library Design & Programmable Logic/I/O Cells	**[12 Hrs.]**
ASIC Library Design: Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multistage cells, Optimum delay and number of stages, library cell design. **Programmable ASIC Logic Cells:** MUX as Boolean function generators, Acted ACT: ACT 1, ACT 2 and ACT 3 Logic Modules, Xilinx LCA: XC3000 CLB, Altera FLEX and MAX, Programmable ASIC I/O Cells: Xilinx and Altera I/O Block.	
UNIT–III: Design Entry, Netlisting & Partitioning for ASIC Construction	**[12 Hrs.]**
Low-level design entry: Schematic entry: Hierarchical design, The cell library, Names, Schematic Icons & Symbols, Nets, Schematic Entry for ASICs, Connections, vectored instances & buses, Edit in place, attributes, Netlist screener. **ASIC Construction:** Physical Design, CAD Tools System partitioning, Estimating ASIC size. **Partitioning:** Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms.	
UNIT–IV: Floor planning & Timing-Driven Placement	**[12 Hrs.]**
Floor planning and placement: Goals and objectives, Measurement of delay in Floor planning, Floor planning tools, Channel definition, I/O and Power planning and Clock planning. **Placement:** Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Time driven placement methods, Physical Design Flow.	
UNIT–V: Global/Detailed Routing, Extraction & DRC	**[12 Hrs.]**
Routing: Global Routing: Goals and objectives, Global Routing Methods, Global routing between blocks, Back-annotation. Detailed Routing: Goals and objectives, Measurement of Channel Density, Left-Edge Algorithm, Area-Routing Algorithms, Multilevel routing, Timing –Driven detailed routing, Final routing steps, Special Routing, Circuit extraction and DRC.	

Text Books

S.N	Title	Authors	Edition	Publisher
1	Application-Specific Integrated Circuits	M. J. S. Smith	1st, 1997 (reprints acceptable)	Addison-Wesley / Pearson
2	Algorithms for VLSI Physical Design Automation	Naveed A. Sherwani	3rd, 1999 (or later)	Springer (Kluwer)

Reference Books

S.N	Title	Authors	Edition	Publisher
1	CMOS VLSI Design: A Circuits and Systems Perspective	Neil H. E. Weste, David Harris	4th or later	Pearson
2	Synthesis and Optimization of Digital Circuits	Giovanni De Micheli	1st, 1994	McGraw-Hill

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Course Code	Course Name	Th	Tu	Pr	Credits	Evaluation		
						CA	ESE	Total
25ES105T(ii)	Program Elective- I Robotics & Automation	4	-	-	4	40	60	100

Course Objectives	Course Outcomes
1. Provide an understanding of the history, components, and classifications of robots along with industrial automation systems. 2. Explore the kinematics, dynamics, and control methods for robotic manipulators and motion planning. 3. Introduce sensors, perception techniques, and communication networks used in automation and robotics. 4. Examine advanced topics such as collaborative robots, SLAM, safety standards, and future trends through case studies and capstone projects.	After successful completion of the course, students will be able to: 1. Explain robotic architectures, components, and industry automation systems including cyber-physical integration. 2. Apply kinematics, dynamics, and control techniques for motion planning and trajectory tracking in robotic systems. 3. Integrate sensors, perception algorithms, and communication protocols for automated material handling and navigation. 4. Design, simulate, and implement advanced robotic solutions focusing on safety, collaboration, and industry-specific applications.

UNIT- I: Fundamentals of Robotics, Automation & Industry Integration	**[12 Hrs]**
History and evolution of robotics; classification of robots based on applications and kinematics,Overview of robotic system components: actuators, sensors, controllers, end-effectors.Degrees of freedom (DOF), workspace analysis, joint types, and common robotic configurations (Cartesian, cylindrical, SCARA, articulated, delta).Basics of industrial automation: PLCs, SCADA systems, CNC machining, flexible manufacturing systems (FMS).Industry 4.0 trends: cyber-physical systems, IoT integration, real-time data analytics in robotics.	
UNIT-II : Kinematics, Dynamics & Motion Planning for Robotics	**[12 Hrs]**
Forward and inverse kinematics for robotic manipulators; analytical and numerical approaches, Jacobian matrices, singularity analysis, and redundancy resolution.Dynamics formulations: Euler-Lagrange equations, Newton-Euler methods,Trajectory planning in joint space and task space with interpolation methods.Control methods: PID control, computed torque control, hybrid force/position control strategies.Motion control challenges in CNC machines and industrial robots	
UNIT-III: Sensors, Perception & Communication in Automation Systems	**[12 Hrs]**
Overview of sensors used in robotics: encoders, force/torque sensors, vision sensors, and proximity sensors,Sensor fusion methods including Extended Kalman Filter (EKF) and Particle Filter techniques for localization,Machine vision applications: image processing, object detection, defect inspection, and AI-driven perception,Automation systems integration: conveyors, Automated Guided Vehicles (AGVs), robotic material handling, and warehouse automation,Networking protocols: fieldbus, industrial Ethernet, OPC-UA for communication and control.	
UNIT-IV: Safety, Reliability & Autonomous Navigation in Robotics	**[12 Hrs]**
Safety standards and functional safety protocols: ISO 10218, ISO 26262, IEC 61508,Fail-safe mechanisms: watchdog timers, fault tolerance, and error recovery, Autonomous navigation techniques: SLAM (Simultaneous Localization and Mapping), path planning algorithms, Emerging trends in robotics: collaborative robots (cobots), humanoids, soft robotics, swarm robotics,AI-driven automation applications across industries: healthcare, agriculture, defense, and service sectors.	
UNIT-V: Advanced Applications, Edge Intelligence & Capstone Project	**[12 Hrs]**
Integration of manipulators, drones, and autonomous systems in real-world applications,Cloud robotics and AI-driven automation architectures for scalable systems,Edge computing solutions: resource-constrained AI, distributed data processing, and real-time decision making,Capstone project planning: requirements gathering, design simulation, implementation, and validation,Case studies from smart factories, defense applications, and autonomous navigation platforms.	

Text Books

S.N	Title	Authors	Edition	Publisher
1	Introduction to Robotics: Mechanics and Control	John J. Craig	4th	Pearson
2	Robotics: Modelling, Planning and Control	Bruno Siciliano, Lorenzo Sciavicco, Luigi Villani, Giuseppe Oriolo	2nd	Springer
3	Modern Robotics: Mechanics, Planning, and Control	Kevin M. Lynch, Frank C. Park	1st	Cambridge University Press

Reference Books

S.N	Title	Authors	Edition	Publisher
1	Robotics, Vision and Control: Fundamental Algorithms in MATLAB	Peter Corke	3rd	Springer
2	Robot Operating System (ROS) for Absolute Beginners	Lentin Joseph	1st	Packt Publishing
3	Safety of Machinery – General Principles for Design – Risk Assessment and Risk Reduction (ISO 12100) / Functional Safety – Road vehicles – ISO 26262	International Standards Organization (ISO)	Latest	ISO / BSI Group