ST. VINCENT PALLOTTI COLLEGE OF ENGINEERING & TECHNOLOGY, NAGPUR

(An autonomous institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech. Scheme of Examination & Syllabus 2024-25

COMPUTER ENGINEERING

SEMESTER III

Sr No	Course Category	Course Code	Course Title	Hours per Week			Credits	Maximum Marks				No. of Hrs for ESE
				L	T	P		Mid-Sem Examination	Continual Assessment	End Sem Examination	Total	
1.	PCC	**24CE301T**	Mathematics for Computer Engineering	**3**	**-**	**-**	**3**	**20**	**20**	**60**	**100**	**3**
2.	PCC	**24CE302T**	Data Structures	**3**	**-**	**-**	**3**	**20**	**20**	**60**	**100**	**3**
3.	PCC	**24CE302P**	Data Structures Lab	**-**	**-**	**2**	**1**	**-**	**25**	**25**	**50**	**-**
4.	PCC	**24CE303T**	Digital Circuits and Fundamentals of Microprocessors	**3**	**-**	**-**	**3**	**20**	**20**	**60**	**100**	**3**
5.	PCC	**24CE303P**	Digital Circuits and Fundamentals of Microprocessors Lab	**-**	**-**	**2**	**1**	**-**	**25**	**25**	**50**	**-**
6.	PCC	**24CE304T**	Computer Architecture	**3**	**-**	**-**	**3**	**20**	**20**	**60**	**100**	**3**
7.	PCC	**24CE305P**	Computer Lab-I	**-**	**-**	**2**	**1**	**-**	**25**	**25**	**50**	**-**
8.	VEC	**24ES301T**	Value Education Course	**3**	**-**	**-**	**3**	**20**	**20**	**60**	**100**	**3**
9.	MDM	**24CE331M**	Indian Cyber Law	**2**	**-**	**-**	**2**	**10**	**10**	**30**	**50**	**1.5**
10.	SEC	**24CE341P**	Career Development - III	**-**	**-**	**2**	**1**	**-**	**50**	**-**	**50**	**-**
11.	ELC	**24CE306P**	Micro Project I*	**-**	**-**	**2**	**1**	**-**	**50**	**-**	**50**	**-**
			Total	**17**	**0**	**10**	**22**	**110**	**260**	**380**	**750**	

*** Field Project or Community engagement project in the major discipline**

		JUNE 2025	NEP 2.1	**Applicable for 2025-26**
Chairman - BoS	**Dean – Academics**	**Date of Release**	**Version**	

THIRD SEMESTER

Course Code	Course Name	Th	Tu	Pr	Credits	Evaluation		
						CA	ESE	Total
24CE301T	Mathematics for Computer Engineering	3	-	-	3	40	60	100

Course Objectives	Course Outcomes
The aim of this course is • To understand the concepts of graph theory and related algorithm concepts. • To understand the concepts of algebraic structures, logic, set theory.	**Students will be able to** • Form truth tables, proving results by truth tables. • Observe the various types of sets, functions and relations. • Recognize definition and properties of algebraic structures. • Apply concepts of graph theory, shortest path algorithms, concepts of trees and minimum spanning tree to solve engineering problems. • Apply counting techniques to solve combinatorial problems.

Unit I : Mathematical logic & Set theory: **[9 Hrs]**
Introduction - Statements and notations, Connectives, Conditional statements and tautologies, Principle of Mathematical Induction, Basic concepts of set theory, Validity of the argument, Operations on sets, Power set.

Unit II : Relation & Function: **[9 Hrs]**
Relation, types of relation, Matrix & Graphical representation of relation, Composition of relation, Partial ordering, Partial ordered set, Hasse diagram. Definition and types of function, Composition of function, Characteristic function.

Unit III : Algebraic Structure & Lattices: **[9 Hrs]**
Binary operations, Group, Problems on groups, subgroup, Lagrange's theorem. Ring, Commutative ring, Ring with unity, Ring with zero divisor, Integral domain, and field. Lattice.

Unit IV : Graph theory & Trees: **[9 Hrs]**
Types of graphs, Isomorphic digraph, Paths and circuits, Reachability and connectedness, Matrix representation of graphs, Euler path and Euler circuit.
Tree: Trees, Binary tree, spanning tree, Weighted graphs, Prim's algorithm, Kruskal's algorithm.

Unit V : Combinatorics : **[9 Hrs]**
Generating Functions, Recurrence Relations, Counting: Permutations & Combinations, Pigeonhole Principle with Simple Applications.

Text Books

S.N	Title	Authors	Edition	Publisher
1.	Discrete Mathematical Structures	Kolman, Busby & Ross		PHI
2.	Discrete Mathematical Structures with Applications to Computer Science	Tremblay & Manohar		Tata McGraw- Hill.
3.	Discrete mathematics	Swapan kumar Sarkar		S. Chand publications

Reference Books

S.N	Title	Authors	Edition	Publisher
1.	Discrete Maths for Computer Scientists & Mathematicians	Mott, Kandel, Baker		Pearson
2.	Discrete Mathematics	Lipschutz		McGraw Hill Professional
3.	Elements of Discrete Mathematics	C. L. Liu		McGraw Hill Education India.

THIRD SEMESTER

Course Code	Course Name	Th	Tu	Pr	Credits	Evaluation		
						CA	ESE	Total
24CE302T	Data Structure	3	-	-	3	40	60	100

Course Objectives	Course Outcomes
This course is intended ● To provide knowledge of basic concepts in data structures and algorithms. ● To choose the appropriate data structure and algorithm design method for a specified application. ● To efficiently implement the different data structures and solutions for specific problems	**Students will be able to** ● To understand the basic concept of data structures, time complexity and analyse the various sorting and searching algorithms. ● To implement dynamic data structures like singly, doubly and circular linked list. ● Apply the different linear data structures like stack and queue to various computing problems. ● Implement different types of trees and apply them to problem solution. ● Demonstrate the representation of graphs and their applications in real life problem

Unit I **[9 Hrs]**

Introduction: Concept of Data structures, Time and space analysis of algorithms, Big oh and theta notations and omega notations, Average, best and worst case analysis,

Searching and sorting techniques: Linear search, Binary search, Insertion sort, selection sort, Bubble Sort, radix Sort, Merge Sort, and Quick Sort.

Unit II **[9 Hrs]**

Linked Lists: Singly linked list, Implementation of linked list using static and dynamic memory allocation, operations on linked list, polynomial representations and manipulations using linked list, circular linked list, doubly linked list, Generalized list, sparse matrix.

Unit III **[9 Hrs]**

Stack and Queue : Array representation of stacks, Implementation of stack using linked lists, Queues, Dequeue, Circular queue, Polish notation, Applications of stack & queue : Conversion from Infix to Postfix, Evaluation of post fix expressions, Priority Queues.

Unit IV **[9 Hrs]**

Trees: Basic Terminology, Basic trees, Binary tree representations, threaded storage representation, binary tree traversals, binary search trees, Application of trees. Preliminary treatment of AVL Trees, B+ Trees.

Unit V **[9 Hrs]**

Graphs: Definition & terminology, Graph representation: matrix representation of Graph, List representation, Breadth First Search, Depth First Search, Spanning trees, Shortest path algorithm, topological sorting.

Text Books

S.N	Title	Authors	Edition	Publisher
1	Data Structure & Program Design in C	Kruse, Leung, Tondo		PHI
2	Data Structures using C	Tanenbaum		Pearson Education
3	Data structure and Algorithm	Lafore		BPB Publication

Reference Books

S.N	Title	Authors	Edition	Publisher
1	Fundamentals of Data Structure	Horowitz and Sahani		CBS Publications
2	Schaum's outline: Data Structures	Seymour Lipschutz		Tata Mc Graw Hill
3	An Introduction to DS with applications	Trembley and sorenson		Mc Graw Hill

THIRD SEMESTER

Course Code	Course Name	Th	Tu	Pr	Credits	Evaluation		
						CA	ESE	Total
24CE302P	Data Structures Lab	-	-	2	1	25	25	50

Course Objectives	Course Outcomes
This course is intended ● To emphasize the application of data structures in developing and implementing efficient programs and algorithm	**Students will be able to** ● Select appropriate data structures as applied to specified problem definition ● Implement linear and non-linear data structures. ● Implement operations like searching, insertion, and deletion, traversing mechanism etc. on various data structures

Expt. No.	Title of the experiment
1	To design and implement basic C program using arrays & structures.
2	To implement a Menu driven program for linear & binary search methods and demonstrate their constraints.
3	To implement a Menu driven program for Sorting methods and analyze their performances.
4	To implement a Program to demonstrate the working of a stack.
5	To implement a Program to demonstrate the working of a Queue.
6	To implement a Program to apply the concepts of linked list.
7	To implement the nonlinear data structure binary tree.
8	To implement BFS and DFS in graph.

Text Books

S.N	Title	Authors	Edition	Publisher
1	Data Structure & Program Design in C	Kruse, Leung, Tondo		PHI
2	Data Structures using C	Tanenbaum		Pearson Education
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S.N	Title	Authors	Edition	Publisher
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THIRD SEMESTER

Course Code	Course Name	Th	Tu	Pr	Credits	Evaluation		
						CA	ESE	Total
24CE303T	Digital Circuits and Fundamentals of Microprocessors	3	-	-	3	40	60	100

Course Objectives	Course Outcomes
This course is intended ● To acquire the basic knowledge of digital logic levels and application of knowledge to understand digital electronics circuits. ● To impart the knowledge of designing Digital Circuits. ● To understand 8086 microprocessor concepts and architecture.	**Students will be able to** ● Represent numerical values in various number systems and will demonstrate the knowledge of logic gates (AND, OR, NAND, NOR, XOR, XNOR), Boolean algebra, De-Morgan's Theorems and Karnaugh map. ● Analyze and design digital combinational circuits. ● Analyze and design sequential digital circuits. ● Analyze & Design Shift Registers and Counters. ● Describe the architecture & organization of 8086 microprocessor.

Unit I **[9 Hrs]**

Number Systems & Code Conversion: Number Systems & Code conversion, Boolean Algebra & Logic Gates, Truth Tables, Universal Gates, Simplification of Boolean functions, SOP and POS methods –Simplification of Boolean functions using K- maps (up to 4 Variable K-map), Signed and Unsigned Binary Numbers.

Unit II **[9 Hrs]**

Combinational Circuits: Adders & Subtractors, BCD Adder & Subtractor, Carry Look ahead adder, Multiplexers, De-multiplexers, Encoders, Decoders.

Unit III **[9 Hrs]**

Sequential Circuits: RS, Clocked RS, D, JK, T Flip-Flops, Master Slave JK, Conversion of Flip Flops from one type to another.

Unit IV **[9 Hrs]**

Shift Registers, Types of Shift Registers, Counters, Ripple Counter, Synchronous Counters, Asynchronous Counters, Up-Down Counter, Decade & BCD Counters.

Unit V **[9 Hrs]**

Fundamentals of 8086 Microprocessors: 8086 microprocessor, Functional Diagram, register organization 8086, Flag register of 8086 and its functions, Addressing modes of 8086, Pin diagram of 8086, Minimum mode & Maximum mode operation of 8086, Interrupts in 8086.

Text Books

S. N.	Title	Authors	Edition	Publisher
1	Digital Design	M. Morris Mano, Michael D. Ciletti	5th Edition	Pearson Education
2	Digital Electronics: Principles, Devices and Applications	Anil K. Maini		John Wiley & Sons, Ltd
3	Microprocessor and Microcontrollers	N. Senthil Kumar, M. Saravanan, S Jeevanathan		Oxford Publishers

Reference Books

S. N.	Title	Authors	Edition	Publisher
1	Modern Digital Electronics	Jain R.P	4th Edition	TMGH
2	Digital Fundamentals – A Systems Approach	Thomas L. Floyd		Pearson
3	Microprocessors and Interfacing.	D.V.Hall,	2nd Edition	TMGH
4	Advanced Microprocessors and Peripherals	A.K.Ray Bhurchandi K.	2nd Edition	TMGH

THIRD SEMESTER

Course Code	Course Name	Th	Tu	Pr	Credits	Evaluation		
						CA	ESE	Total
24CE303P	Digital Circuits and Fundamentals of Microprocessors Lab	-	-	2	1	25	25	50

Course Objectives	Course Outcomes
This course is intended • To introduce the basic concepts and laws involved in the Boolean algebra and logic families and digital circuits. • To familiarize with the different logic gates, combinational and sequential circuits utilized in the different digital circuits and systems. • To introduces basic instruction of microprocessor.	**Students will be able to** • Understand the combinational circuits using logic gates. • Design arithmetic and logical Circuit • Demonstrate understanding of flip-flops & sequential circuits. • Understand the basic fundamentals of 8086 Microprocessor

Expt. No.	Title of the experiment
1	To verify the truth table of different logic gates.
2	To study and verify the NAND & NOR gates as universal gates.
3	To study and verify De Morgan's Law
4	To study and verify truth table of Half adder and Full Adder using two half adder.
5	To study and verify truth table of Multiplexer & Demultiplexer.
6	To study and verify truth table of different flip flops.
7	To study and verify truth table of Seven Segment Display Decoder.
8	To study and verify 4 bit ripple counter.
9	Write and execute an ALP for addition & Subtraction of two 16 bit numbers.
10	Write and execute an ALP to find 1's complement of 16 bit a number

S.N	Title	Authors	Edition	Publisher
1	Modern Digital Electronics	Jain R.P	4th Edition	TMGH
2	Digital Fundamentals – A Systems Approach	Thomas L. Floyd		Pearson
3	Fundamentals of Logic Design	Charles H. Roth	5th Edition	Cengage Learning
4	Microprocessors and Interfacing.	D.V.Hall,	2nd Edition	TMGH

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Chairman - BoS	**Dean – Academics**	**Date of Release**	**Version**	

THIRD SEMESTER

Course Code	Course Name	Th	Tu	Pr	Credits	Evaluation		
						CA	ESE	Total
24CE304T	Computer Architecture	3	-	-	3	40	60	100

Course Objectives	Course Outcomes
This course is intended ● To provide understanding of design of Computer Architecture and organization. ● To provide understanding of issues involved in design ofcontrol unit. ● To understand the concepts of memory organization andits interfacing.	**Students will be able to** ● Analyze and describe differentcomputer architectures. ● Solve various computer arithmeticproblems ● Analyze the complete execution of instructionsusing different control units. ● Understand I/O device interfacing. ● Understand computer memory hierarchy and multiprocessor systems

Unit I **[9 Hrs]**

Basic structure of computers: A Brief History of computers Designing for Performance Von Neumann Architecture, Computer Components, Interconnection Structures, Bus Interconnection, Addressing modes, Instruction Set Architecture (Instruction set based classification of processor i.e. RISC, CISC,RISC vs CISC Comparison).

Unit II **[9 Hrs]**

Arithmetic Unit : Addition & subtraction of signed numbers, Booths Multiplication Algorithm, Restoring Division Algorithm, Non - Restoring Division Algorithm, Floating point operations

[9 Hrs]

Unit III

Processing unit : Machine Instruction characteristics, types of operands, types of operations, Instruction formats, Instruction types, Processor organization, Register Organization

Control unit : Hardwired control unit, Microprogrammed control unit

Unit IV **[9 Hrs]**

Pipelining : Instruction cycles, Instruction Pipelining, Hazards, Multiple bus organization

I/O Organization: Input/output Systems, Memory Mapped I/O, I/O Mapped I/O, Programmed I/O, Interrupt Driven I/O, Direct Memory Access (DMA)

Unit V

[9 Hrs]

Memory Systems: Memory Hierarchy, Cache memory, Main Memory, Virtual memory, Secondary storage - RAID, Memory Interleaving **Multiprocessor Systems :** Basic concept, Shared memory multiprocessor systems

Text Books

S.N	Title	Authors	Edition	Publisher
1	Computer Organization & Architecture	William stalkings	8th Edition	Prentice Hall
2	Computer Organization	Carl Hamacher	5th Edition	McGraw Hill

Reference Books

S.N	Title	Authors	Edition	Publisher
1	Computer Architecture: A QuantitativeApproach	John L. Hennessy, David A. Patterson,	6th Edition	Elsevier Science
2	Computer organization	J. P. Hayes	5th Edition	Tata McGraw

THIRD SEMESTER

Course Code	Course Name	Th	Tu	Pr	Credits	Evaluation		
						CA	ESE	Total
24CE305P	Computer Lab- I	-	-	2	1	25	25	50

Course Objectives	Course Outcomes
This course is intended ● To provide understanding of basic problem solving using competitive programming ● To enhance the ability for complex problem solving using competitive programming	**Students will be able to** ● Explore and implement the competitive programming concepts of Basic programming ● Explore and implement the advanced concepts of competitive programming

Expt. No.	Title of the experiment
1	To explore the competitive programming examples based on Basic Programming
2	To explore the competitive programming examples based on Array
3	To explore the competitive programming examples based on Data Structure
4	To explore the competitive programming examples based on Strings
5	To explore the competitive programming examples based on Sorting
6	To explore the competitive programming examples based on Binary Search
7	To explore the competitive programming examples based on Maths

Text Books

S.N	Title	Authors	Edition	Publisher
1	Let us C	Yashwant Kanetkar		BPB Publication
2	Python Programming: A PracticalApproach	Vijay Kumar Sharma, VimalKumar,SwatiSharma,ShashwatPathak		CRC Press

THIRD SEMESTER

Course Code	Course Name	Th	Tu	Pr	Credits	Evaluation		
						CA	ESE	Total
24ES301T	Value Education Course-I	2	-	-	2	20	30	50

Course Objectives	Course Outcomes
This course is intended • To develop a holistic perspective through self-exploration and development of clarity about harmony between self, family, society and nature.	**Students will be able to** ● Demonstrate awareness about concepts like self-exploration & natural acceptance. ● Understand concepts of aspirations and Happiness. ● Develop clarity of harmony and health in human being. ● Discuss concepts of conservation of nature and harmony in nature/existence and re-usability.

Unit I : Introduction to Self-Exploration **[7 Hrs]**

- Purpose & motivation for studying universal human values.
- Self-Exploration–what is it? - Its content and process.
- 'Natural Acceptance' and Experiential Validation- as the process for self-exploration.

[7 Hrs]

Unit II: Understanding Happiness and Prosperity

- Understanding Happiness and Prosperity correctly.
- Continuous Happiness and Prosperity- A look at basic Human Aspirations.
- Right understanding, Relationship and Physical Facility.
- Method to fulfill the above human aspirations: understanding and living in harmony at various levels.

[8 Hrs]

Unit III: Understanding Harmony in human being

- Understanding human being as a co-existence of the sentient 'I' and the material 'Body'.
- Understanding the needs of Self ('I') and 'Body' - happiness and physical facility.
- Understanding the Body as an instrument of 'I' (I being the doer, seer and enjoyer).
- Understanding the characteristics and activities of 'I' and harmony in 'I'.
- Understanding the harmony of I with the Body: Sanyam and Health.

[8 Hrs]

Unit IV: Co-existing with nature

- Understanding the harmony in Nature.
- Interconnection and mutual fulfillment among the four orders of nature- recyclability and self-regulation in nature.
- Understanding Existence as Coexistence of mutually interacting units in all-pervasive space.
- Holistic perception of harmony at all levels of existence.
- Pollution, depletion of resources and role of technology.

Text Books

S.N	Title	Authors	Edition	Publisher
1	Human Values and Professional Ethics	Gaur, Sangal, Bagaria	2010	Excel Books, New Delhi

Reference Books

S.N	Title	Authors	Edition	Publisher
1	Jeevan Vidya: Ek Parichaya	A. Nagaraj	1999	Jeevan Vidya Prakashan, Amarkantak
2	Human Values	A.N. Tripathi	2004	New Age Intl. Publishers, New Delhi
3	The Story of My Experiments with Truth	M.K.Gandhi	2009	Fingerprint! Publishers

Online Resources

1	https://fdp-si.aicte-india.org/UHV-II%20Class%20Note.php
2	https://fdp-si.aicte-india.org/UHV-II_Lectures_PPTs.php

THIRD SEMESTER

Course Code	Course Name	Th	Tu	Pr	Credits	Evaluation		
						CA	ESE	Total
24CE331M	MDM-I Indian Cyber law	2	-	-	2	20	30	50

Course Objectives	Course Outcomes
The aim of this course is • To be a safety net against online data predators • To ensure justice for cybercrime victims • To prevent debit card or credit card fraud	**Students will be able to** • Identify nexus between e-commerce and cyber laws and Examine the legal framework of e-governance mechanism in India. • Analyze legal liabilities towards changing environment of cyber space. • Formulate implications of cyber offences for Intellectual property rights

Unit I **[8 Hrs]**

Introduction to Cyber Laws – In Indian Context:

Information Technology Act 2000, Amendments made in the Indian ITA 2000, Positive Aspects of the ITA 2000, The Weak Areas of the ITA 2000, Challenges to Indian Law and Cybercrime Scenario in India, Consequences of Not Addressing the Weakness in Information Technology Act Amendments to the Indian ITA 2008, Impact of IT Act Amendments Impact Information Technology Organizations, Cybercrime and Punishment.

Unit II **[8 Hrs]**

Internet and the Protection of Software Copyright:

Open Source, Reverse Engineering Trademark Issues in Cyber Space: - Domain Name, the ICANN Uniform Domain Name Dispute Resolution Policy.

Unit III **[8 Hrs]**

A IPR in Cyber Space: -Patents in Digital Technology, Copy Rights in Digital Space, WIPO Internet Treaties, Trademark Online IP Related Cyber Crimes: - Introduction, Essential Ingredients of Crime, Types of Internet Crimes, Cyber Crime and IPR.

Text Books

S.N	Title	Authors	Edition	Publisher
1	Cyber Laws	Yatindra Singh	2016	Universal Law Publishing Co.Pvt.Ltd
2	Law Relating to Computers Internet & E-Commerce	Nandan Kamath	IInd	Universal Law Publishing Co.Pvt.Ltd

Reference Books

S.N	Title	Authors	Edition	Publisher
1	Social, ethical and policy implication of Information Technology.	Linda Brennan and Victoria Johnson	-	Information Science Publishing
2	International Domain Name Law ICANN at the UDRP	David Lindsy	2017	Hart Publishing